Gokul Subramanian Ravi *Curriculum Vitae*

Contact Information

University Of Wisconsin-Madison
Electrical and Computer Engineering
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Research Interests

Computer Architecture and Systems:
Microarchitecture. ML-assisted system design. Cross-layer optimization. Quantum Computing. Approximate Computing.

Dissertation Research

Vertical integration in classical computers with specific focus on the system's clock. My contributions demystify the computer's abstraction of the clock by understanding the clocking system's structural, functional and differential characteristics; and leveraging them via optimizations across multiple layers of the system stack. Contributions to spatial architectures, reconfigurable computing, out-of-order core microarchitecture, approximation computing, network-on-chip and application of ML.

Education Background

University of Wisconsin-Madison August 2020 (expected)
- PhD Candidate in Electrical and Computer Engineering. GPA: 3.97/4.0
- Adviser: Prof. Mikko Lipasti
- Thesis: *Demystifying the computer's clock abstraction for system-wide benefits*

Birla Institute of Technology and Science, Pilani May 2012
- B.E. (Hons.) Electronics and Instrumentation Engineering. GPA: 3.6/4.0

Publications

[1] Gokul Subramanian Ravi, Ramon Bertran, Pradip Bose, and Mikko Lipasti. "ML-Assisted Co-design of Code and Architecture", 2020 (**Under Submission 2020**)
Guarantee aggressive SLAs with ML-assisted software-hardware integration, via the co-design of workloads and architecture.

[2] Gokul Subramanian Ravi, Tushar Krishna, and Mikko Lipasti. "Modular Design for Transparent Network Traversal", 2020 (**Under Submission 2020**)
Source to destination network traversal as a single multi-cycle "long-hop", bypassing the quantization effects of intermediate routers via transparent flow.

[3] Rahul Singh, Gokul Subramanian Ravi, Mikko Lipasti, and Joshua San Miguel. "Value Locality based Approximation with ODIN", to appear in IEEE Computer Architecture Letters, 2020 (**CAL 2020**)
Eliminating load-compute-store slices by evaluating output redundancy.

[4] Gokul Subramanian Ravi, Joshua San Miguel, and Mikko Lipasti. "Synergic HW-SW Architecture for Fine-Grained Spatio-Temporal Approximation", to appear in ACM Transactions on Architecture and Code Optimization, 2020 (**TACO 2020**)
Hardware approximation via timing approximation and dynamic pre-L1 load approximation + Hardware-cognizant approximation tuning + Synergic benefits.

[5] Gokul Subramanian Ravi and Mikko H. Lipasti, "Recycling Data Slack in Out-of-Order Cores," 2019 IEEE International Symposium on High Performance Computer Architecture (**HPCA 2019**)
Aggressively recycles unique per-operation data slack via transparent datapaths within an OOO core.

[6] Gokul Subramanian Ravi, Tushar Krishna, and Mikko Lipasti. "McMahon: Minimum-cycle Maximum-hop network.", Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems co-located w/ HiPEAC 2019 (**AISTECS 2019**)

Source to destination network traversal as a single multi-cycle "long-hop", bypassing the quantization effects of intermediate routers via transparent flow.

[7] Gokul Subramanian Ravi and Mikko H. Lipasti. 2018. "Aggressive Slack Recycling via Transparent Pipelines". In Proceedings of the International Symposium on Low Power Electronics and Design (**ISLPED 2018**)
Timing speculation to cater to the average slack across asynchronous operations rather than the slack of the most critical operation.

[8] Gokul Subramanian Ravi and Mikko Lipasti. "Accelerating Approximations via Slack Recycling.", Workshop on Approximate Computing co-located w/ ASPLOS 2018 (**WAX 2018**)
Hardware approximation via timing approximation.

[9] Gokul Subramanian Ravi and Mikko H. Lipasti. 2017. "CHARSTAR: Clock Hierarchy Aware Resource Scaling in Tiled ARchitectures". In Proceedings of the 44th Annual International Symposium on Computer Architecture (**ISCA 2017**)
Using ML to make resource+frequency scaling in tiled architectures to be clock hierarchy aware.

[10] Gokul Subramanian Ravi and Mikko H. Lipasti, "Timing Speculation in Multi-Cycle Data Paths," in IEEE Computer Architecture Letters, vol. 16, Jan.-June 2017 (**CAL 2017**)
Timing speculation to cater to the average slack across asynchronous operations rather than the slack of the most critical operation.

[11] Hyeran Jeon, Gokul Subramanian Ravi, Nam Sung Kim, and Murali Annavaram. 2015. "GPU register file virtualization". In Proceedings of the 48th International Symposium on Microarchitecture (**MICRO 2015**)
Allows multiple warps to share physical registers by virtualizing the register file.

[12] Gokul Subramanian Ravi, Aditya Narayan, and Vinod Kumar Chaubey. 2011. "FPGA Implementation of Viterbi Algorithm and Adaptive Viterbi Algorithm for normal and turbo coded data". In Proceedings of the National Conference for VLSI Design and Embedded Systems. 2011 (**NCVDES 2011**)
Design space exploration and implementation of different algorithms and for different styles of encoding.

Patents

1. "Hardware Assisted Fine-Grained Data Movement". Muhammad Amber Hassan et al. Patent pending. 2020 (**AMD Research 2020**)
2. "Computer Architecture Allowing Recycling of Instruction Slack Time". Gokul Subramanian Ravi and Mikko Lipasti. Patent pending. 2019 (**UW-Madison 2019**)

Talks

1. "Vertical Integration in Computing Systems: Demystifying the Computer's Clock Abstraction". Three Minute Thesis Competition, UW-Madison, 2019 (**3MT 2019**)
2. "Vertical Integration in Computing Systems: Demystifying the Computer's Clock Abstraction". Invited Talk at Rising Stars in Computer Architecture Workshop, Georgia Tech, 2019 (**RISC-A 2019**)
3. "Vertical Integration in Computing Systems: Demystifying the Computer's Clock Abstraction". UW-Madison Computer Engineering Seminar, 2019 (**CE-Seminar 2019**)
4. "TNT: Modular Design for Transparent Network Traversal". UW-Madison Computer Architecture Affiliates, 2019 (**Affiliates 2019**)
5. "Exploiting Timing Guardbands for Accurate and Approximate Computing". Invited Talk at IBM TJ Watson Research Center, NY, 2019 (**IBM 2019**)

6. "Recycling Data Slack in Out-Of-Order Cores". 25th IEEE International Symposium on High-Performance Computer Architecture, 2019 (**HPCA 2019**)
7. "McMahon: Minimum-cycle Maximum-hop network". Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems co-located w/ HiPEAC, 2019 (**AISTECS 2019**)
8. "SHASTA and other short stories". UW-Madison Computer Engineering Seminar, 2018 (**CE-Seminar 2018**)
9. "Software-Hardware Approximation for Sustainable Timing Approximation". UW-Madison Computer Architecture Affiliates, 2018 (**Affiliates 2018**)
10. "Aggressive Slack Recycling via Transparent Pipelines". ACM/IEEE International Symposium on Low Power Electronics and Design, 2018 (**ISLPED 2018**)
11. "Axl: Accelerating Approximations via Slack Recycling". Workshop on Approximate Computing co-located w/ ASPLOS, 2018 (**WAX 2018**)
12. "Slack Recycling in Processor Architectures ". UW-Madison Computer Engineering Seminar, 2017 (**CE-Seminar 2017**)
13. "Recycling Data Slack in OOO Cores". UW-Madison Computer Architecture Affiliates, 2017 (**Affiliates 2017**)
14. "Clock Hierarchy Aware Resource Scaling in Tiled Architectures". Invited Talk at Google, CA, 2017 (**Google 2017**)
15. "CHARSTAR: Clock Hierarchy Aware Resource Scaling in Tiled Architectures". 44th ACM/IEEE International Symposium on Computer Architecture, 2017, presented by Prof. Lipasti (**ISCA 2017**)
16. "Timing Speculation in Multi-Cycle Data Paths". UW-Madison Computer Architecture Affiliates, 2016 (**Affiliates 2016**)
17. "Timing Speculation in Multi-Cycle Data Paths". ARM Research Summit, 2016, presented by Prof. Lipasti (**ARM 2016**)
18. "GPU Register File Virtualization". 48th Annual IEEE/ACM International Symposium on Microarchitecture, 2015, presented by Hyeran Jeon (**MICRO 2015**)
19. "Spatiotemporal Adaptivity in Tiled Architectures". UW-Madison Computer Architecture Affiliates, 2015 (**Affiliates 2015**)
20. "FPGA Implementation of Viterbi Algorithm and Adaptive Viterbi Algorithm for normal and turbo coded data". National Conference for VLSI Design and Embedded Systems, 2011 (**NCVDES 2011**)

Posters

1. "ML-Assisted Co-design of Code and Architecture". UW-Madison Computer Architecture Affiliates, 2019 (**Affiliates 2019**)
2. "TNT: Modular Design for Transparent Network Traversal". UW-Madison Computer Architecture Affiliates, 2019 (**Affiliates 2019**)
3. "Clocking the clock: Tackling the limiting impact of clocks on synchronous processor designs". ARM Research Summit, 2019 (**ARM 2019**)
4. "Software-Hardware Approximation for Sustainable Timing Approximation". UW-Madison Computer Architecture Affiliates, 2018 (**Affiliates 2018**)
5. "Recycling Data Slack in Out-of-order Cores". UW-Madison Computer Architecture Affiliates, 2017 (**Affiliates 2017**)

6. "Clock Hierarchy Aware Resource Scaling in Tiled Architectures". UW-Madison Computer Architecture Affiliates, 2017 (**Affiliates 2017**)
7. "Timing Speculation in Multi-Cycle Data Paths". UW-Madison Computer Architecture Affiliates, 2016 (**Affiliates 2016**)
8. "Spatio-temporal Adaptivity in Tiled Architectures". UW-Madison Computer Architecture Affiliates, 2015 (**Affiliates 2015**)

Research Experience

Graduate Research Assistant (UW-Madison) Sep 2014 - Present
- Advisor: Prof. Mikko Lipasti
- PhD dissertation research

Graduate Research Assistant (UW-Madison) Sep 2013 - Aug 2014
- Advisor: Prof. Nam Sung Kim
- Technological optimization for heterogeneous architectures

Undergraduate Research Assistant (BITS Pilani) Fall 2011
- Advisor: Prof. Vinod Kumar Chaubey
- FPGA implementation of communication algorithms

Undergraduate Research Assistant (BITS/CEERI Pilani) Fall 2011
- Advisor: Chief Scientist A.S.Mandal
- Analysis of the Harris Corner Detection Algorithm

Teaching Experience

Advanced Computer Architecture - 1 (UW-M ECE/CS 752) Spring 2019
- Taught by: Prof. Joshua San Miguel
- Role: Guest Lecturer
- Lecture on impact of clock cycle slack on modern processors, for graduate students.

Introduction to Computer Architecture (UW-M ECE/CS 552) Spring 2018
- Taught by: Prof. Mikko Lipasti
- Role: Teaching Assistant
- Conducted tutorials and discussions for graduate students and seniors. Primarily responsible for the course project, designing a 5-stage InOrder pipeline in Verilog. Gave occasional lectures. Aided with regular lectures, setting exams and grading.
- Single TA managing 100+ students.

Introduction to Computer Architecture (UW-M ECE/CS 552) Fall 2017
- Taught by: Prof. Yu Hen Hu
- Role: Teaching Assistant
- Conducted tutorials and discussions for graduate students and seniors. Primarily responsible for the course project, designing a 5-stage InOrder pipeline in Verilog. Gave occasional lectures. Aided with regular lectures, setting exams and grading.
- Single TA managing 50+ students.

Microelectronics (BITS, Pilani) Fall 2011
- Role: Professional Assistant
- Tutoring juniors in concepts and use of tools - Eldo SPICE, Cadence Spectre, ModelSim.

Circuits and Signals (BITS, Pilani) Spring 2011
- Role: Professional Assistant
- Tutoring sophomores in the class, assignments and lab work which included course fundamentals, problem solving, Matlab etc.

Computer Programming (BITS, Pilani) Spring 2011
- Role: Professional Assistant
- Tutoring freshmen in C and Unix programming.

Industry/Lab Experience

AMD Research (Austin, TX) Summer 2016
- Research Intern, mentored by Dr. Bradford Beckmann.
- Worked on task scheduling and task synchronization on GPUs.
- Optimized coherence protocols and implemented synchronization under Release Consistency.
- Developed optimized scheduling algorithms for improving concurrency and data sharing.

Qualcomm (Santa Clara, CA) Summer 2014
- Engineering Intern, mentored by Mr. Edmond Cote.
- Designed debug bus checker for units of the GPU.
- Developed performance counters for multiple units.
- Designed a scan chain for post silicon verification.

NVIDIA (Bangalore, India) 2012-2013
- ASIC Design Engineer, managed by Mr. Atul Kalambur.
- Worked on full chip performance verification for Tegra SOCs.
- Analyzed the performance of GPU, PCIE, video decode engine, 2D graphics engine and their combined stress on the central memory controller for different Tegra chips.
- Developed performance infrastructure for the entire SOC.

NVIDIA (Bangalore, India) 2012
- Engineering Intern, managed by Mr. Atul Kalambur.
- System level Performance Verification for Tegra chips.
- Infrastructure development and full chip performance verification focused on external memory card interface and security engine.

Central Electronics Engineering Research Institute (Chennai, India) 2010
- Research Intern, managed by Senior Principal Scientist C. Kumaravelu.
- Implemented a control system for Indian industries using PLS regression, on NI LabVIEW.

Technical Activities

Program Committee
- The Young Architect Workshop 2019
- The Young Architect Workshop 2020

Reviewer
- CASES 2019 (Secondary)
- PACT 2019 (Secondary)

Memberships
- ACM, IEEE, TCCA, SIGARCH

Leadership Positions
- Lead the Computer Architecture Reading Group at UW-Madison over 2018 and 2019.
- ECE GSA member at UW-Madison, 2013-2014.
- Event host and core member of organizing team for EEE Association at the annual nationwide technical gathering hosted by BITS Pilani, 2011.
- Event Manager, Institution of Engineering and Technology (IET), BITS Pilani chapter, 2009-2010.

Skills

Languages: C, C++, Verilog, Python, Bash, Perl, UNIX shell

Software: Modelsim, Design Compiler, HSpice, Cadence Spectre, Matlab, PSoC Designer, NI LabView

Simulators: Gem5, GPGPU-Sim, Gem5-GPU, Aladdin, McPAT, HotSpot, GPUWattch, CACTI, GARNET, Ruby

Relevant Coursework

Advanced Computer Architecture, Programming Languages, Operating Systems, Digital System Design, Electronic Devices, Compilers, Algorithms

Selected Recognition

1. Selected to participate in the Rising Stars in Computer Architecture (RISC-A) Workshop, as a top graduating PhD / Post-doc looking for academic positions. 2019.
2. CHARSTAR's ML-assisted resource management recognized as the state-of-the-art (and used as baseline) by Intel Labs ISCA paper. 2019.
3. GPU Register File Virtualization recognized by Synthesis Lectures on Computer Architecture, General-Purpose Graphics Processor Architectures. 2018.
4. CHARSTAR recognized in the ACM SIGARCH blog post, "Thoughts on ISCA-44". 2017.
5. Awarded Research Assistantship for all semesters of graduate studies, both as a Master's candidate and as a PhD candidate. 2013-Present.
6. Awarded 2nd place in Electronics, at the annual nation-wide technical gathering hosted by IIT Kanpur, for implementing industry process control with PLS regression. 2011.
7. Awarded 2nd place in Physics, at the annual nation-wide technical gathering hosted by BITS Pilani, for building a Van De Graaff generator. 2010.
8. Selected for the Indian National Olympiad for Informatics. 2008.
9. Ranked in the National Science Olympiad and National Cyber Olympiad. 2008.
10. National rank 13 in AMTI National level Mathematics Olympiad. 2008.
11. Ranked 19th in the The Physics Society Physics Olympiad. 2007.