CHARSTAR: Clock Hierarchy Aware Resource Scaling in Tiled ARchitectures

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Power Consumption

- Unclock Dynamic
- Clock Total
- Unclock Leakage
- Power Gating

Resource Cluster

Dynamic Power Consumption
Power Consumption

- Clock Total
- Unclock Dynamic
- Unclock Leakage
- Power Gating

Resource Cluster

CLOCK HIERARCHY!!
Power Consumption

Clock Total

Unclock Dynamic

Unclock Leakage

Clock Gating (Naive)

Power Gating

Dynamic Power Consumption

Resource Cluster

CH-Aware Reconfiguration!!
Power Consumption

- Unclock Dynamic
- Clock Total
- Power Leakage
- Clock Gating (Naïve)

Dynamic Power Consumption

CH-Aware Reconfiguration!!
Power Consumption

- Unclock Total
- Clock Gating (Naive)
- CH-Aware Gating
- Unclock Leakage
- Power Gating

Resource Cluster

CH-Aware Reconfiguration!!
Power Consumption

- Clock
- Total
- CH-Aware
- GaGng
- (Naïve)
- Unclock
- Leakage
- Power
- Gating
- Dynamic

2.2x greater than Naive

CH-Aware Reconfiguration!!

Resource Cluster

Dynamic Power Consumption

Resource Cluster

CH-Aware Reconfiguration!!
Power Consumption

- **Unclock Dynamic**
  - Clock Total
  - CH-Aware Gating
  - Power Gating
  - Unclock Leakage

CH-Aware Reconfiguration!!

- Dynamic Power Consumption: 1.1x greater than PG-only
- Resource Cluster
- CH-Aware Reconfiguration!!

Diagram showing the power consumption breakdown and reconfiguration process.
Power Consumption

- Clock
- Total
- CH-Aware Gating
- Dynamic

CH-Aware Reconfiguration!!

SESSION 3A, TODAY @ 3:10PM  (GRAND EAST L)